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FREQUENCY MULTIPLIER ANALYSIS AND DESIGN USING PUNCH-THROUGH VARACTOR DIODES

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Group 64

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FOR THE COMMANDER

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Administrative Contracting Officer
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ABSTRACT

Punch-through varactor diode frequency multipliers, a type of nonlinear reactive multiplier, can be 100% efficient, theoretically. This report presents a model of a punch-through diode and then analyzes it in the frequency domain. By restricting the currents that flow, the analysis can be reduced to a finite set of equations for any order multiplier. Next, assuming that the diode loss is low enough, diode equations for the specific cases of a doubler and a tripler are developed. The report then adds the necessary circuit elements to give lumped-element circuit designs and design equations for both doublers and triplers. Finally, sample circuits are built using these designs, and design equations are shown along with their performance.

ACKNOWLEDGMENTS

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1. INTRODUCTION

Frequency multipliers are useful circuits in both the RF and microwave regions. For instance, to provide a clean, stable local oscillator (LO) signal at microwave frequencies, the output of a 5- to 100-MHz oscillator is multiplied by a frequency multiplier circuit. The same procedure can be used in a transmitter where the signals are multiplied either before or after the power amplifier. These techniques are preferred over a UHF or microwave oscillator because these higher frequency oscillators are not as quiet or as stable as a frequency-multiplied, low-frequency oscillator.

Two general types of frequency multipliers exist: nonlinear resistive and nonlinear reactive. Nonlinear resistive multipliers are generally impulse multipliers such as comb generators or step recovery diode (SRD) multipliers. When these multipliers are not tuned, they are very broadband circuits. However, they need high drive power and are inefficient. Because their maximum efficiency is $1/N^2$, where N is the order of the multiplier, they are especially inefficient for higher order circuits.

On the other hand, nonlinear reactive multipliers with no series resistance are 100% efficient, and they can be used at lower drive powers. Because the frequency multiplication is based on a nonlinear reactance, these circuits have tuned input and output circuits and often tuned idler circuits as well. Consequently, the tuned circuits cause reactive multipliers to be generally narrowband circuits.

Of the three common types of reactive multipliers, the best known is the abrupt junction varactor diode multiplier that was heavily investigated in the 1950s [1]. Although they can be efficient, their operation is sensitive to their input power level, they need external bias, and they can be hard to stabilize. In the 1960s punch-through diode multipliers were developed [2,3]. Their operation is relatively independent of their input power level, they are self biasing, and they are generally easier to stabilize. Punch-through diodes are known more widely as SRDs, but because punch-through better describes them, they will be referred to as such.

Transistor multipliers were also developed in the 1960s [4,5]. Unlike diode multipliers, they are able to produce gain. Their operation is based on the nonlinear capacitive reactance of the reverse-biased base-collector junction. However, due to the larger complexity of a transistor compared with a diode, they are much harder to analyze.

Though all the previously mentioned reactive multipliers use a nonlinear capacitor, a nonlinear inductor can also be used. In fact the very first frequency multipliers (or frequency changers as they were called then) developed early in this century took advantage of the nonlinear flux density versus magnetic field intensity (B-H) characteristic of iron core inductors [6,7]. Currently, they have fallen out of vogue in the RF and microwave communities, though they are still used in other fields.

This report addresses punch-through diode multipliers only. Though all the work on punch-through diode multipliers was done almost 30 years ago, it was difficult to locate good information about building them. This report tries to rectify that problem. Section 2 presents the theoretical derivation of how these multipliers work; Section 3 gives practical information on how to build them, including lessons that were learned the hard way; and Section 4 shows the results of some multipliers that have been built as a result of this research.

2. THEORETICAL DESCRIPTION

Consider a punch-through diode as a generic nonlinear reactance, in series with a constant resistance, as shown in Figure 1 [1]. For now, no assumptions are made or restrictions placed on the characteristic of the nonlinear elastance.

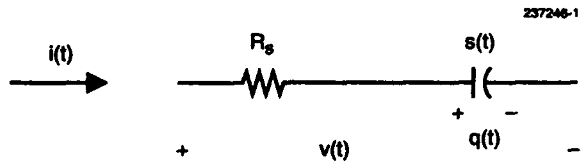

Figure 1. Generic nonlinear capacitor.

Next, the general relationship between the voltage and current in terms of the series resistance and the elastance [1] must be found. Because typically these multipliers are driven with at least 1 mW, the noise can be ignored. Also, for the purposes of the derivation, the initial voltage on the capacitor will be considered zero; hence, the voltage *v(t)* can be written as:

$$v(t) = R_s i(t) + \int s(t) i(t) dt \quad , \tag{1}$$

where

$$s(t) = \frac{dV}{dq}\frac{dq}{dt} \text{ and } i(t) = \frac{dq}{dt} \quad . \tag{2}$$

As usual, *q(t)* is the charge on the capacitor.

This expression is not useful for designing multipliers because the different harmonic voltages and currents are not known. To get Equation (1) into a useful form, the voltage, current, and elastance must be expressed as a Fourier series. At this point, one restriction is imposed—only the first N harmonic currents are allowed to flow. With this in mind, *v(t)*, *i(t)*, and *s(t)* can be expanded as:

$$v(t) = \sum_{k=-\infty}^{\infty} V_k e^{jk\omega_o t} \quad , \tag{3}$$

$$i(t) = \sum_{k=-n}^{n} I_k e^{jk\omega_o t} \quad , \text{ and} \tag{4}$$

$$s(t) = \sum_{k=-\infty}^{\infty} S_k e^{jk\omega_o t} \quad . \tag{5}$$

Because these circuits are real, all the voltages, currents, and elastances are real, which constrains the Fourier coefficients to be:

$$V_{-k} = V_k^*, \quad I_{-k} = I_k^*, \quad \text{and} \quad S_{-k} = S_k^* \quad . \tag{6}$$

Because the desired end result is a generic expression for each harmonic voltage V_k in terms of the currents, I_k; elastances, S_k; and series resistance, R_s; first the Fourier coefficients are calculated in terms of their time domain counterparts. From basic Fourier analysis, these expressions are

$$V_k = \frac{1}{T}\int_t^{t+T} v(x)e^{-jk\omega_o x}dx \ , \tag{7}$$

$$I_k = \frac{1}{T}\int_t^{t+T} i(x)e^{-jk\omega_o x}dx \ , \quad \text{and} \tag{8}$$

$$S_k = \frac{1}{T}\int_t^{t+T} s(x)e^{-jk\omega_o x}dx \quad . \tag{9}$$

Equation (7) gives an expression for each V_k, but to get it in terms of I_k, S_k, and R_s, Equation (1) is substituted into (7) to obtain:

$$V_k = \frac{1}{T}\int_t^{t+T} \left(R_s i(x) + \int s(y)i(y)dy\right)e^{-jk\omega_o x}dx \quad . \tag{10}$$

Nonetheless, the current and elastances are still expressed in the time domain, so Equations (8) and (9) are substituted into (10) to get:

$$V_k = R_s I_k - j\frac{1}{\omega_o T(l+m)}\sum_{l=-n}^{n}\ \sum_{m=-\infty}^{\infty} I_l S_m \int_t^{t+T} e^{j\omega_o x(l+m-k)}dx \quad . \tag{11}$$

Here, the integral is zero except when $m = k - l$, where it is equal to T. Equation (11) can then be written as:

$$V_k = R_s I_k - j\frac{1}{\omega_o k}\sum_{l=-n}^{n} I_l S_{k-l} \tag{12}$$

or in matrix form as:

$$\vec{V} = R_s\vec{I} + [A]\vec{I} \quad , \tag{13}$$

where

$$A_{lk} = -j\frac{S_{k-l}}{\omega_o k} \quad . \tag{14}$$

Equations (12) and (13) relate each harmonic voltage to the harmonic currents, the harmonic elastances, and the series resistance.

Because Equations (12) and (13) are used to determine impedances, the process is easier if all the currents are normalized to I_1. The normalized current D_k is defined:

$$D_k = \frac{I_k}{I_1} \quad . \tag{15}$$

From this equation it is obvious that $D_l = 1$ and $D_{-k} = D_k^*$. Finally, Equations (12) and (13) can be rewritten as:

$$V_k = \left\{ R_s D_k - j\frac{1}{\omega_o k}\sum_{l=-n}^{n} D_l S_{k-l} \right\} I_1 \tag{16}$$

and

$$\vec{V} = \left\{ R_s\vec{D} + [A]\vec{D} \right\} I_1 \quad . \tag{17}$$

With such a general mathematical description of the nonlinear reactance, the reactance can be put in a circuit to give more constraints for Equations (16) and (17), which will enable a general expression for the input and output impedances [8].

Figure 2 shows the input circuit of a general, nonlinear reactive frequency multiplier. The input inductor tunes out the constant or average elastance of the nonlinear reactance, while the higher order terms will appear resistive at the input frequency, resulting in an impedance-matched circuit. Though the contributions by the higher order terms appear resistive, they are not resistors because they are due to nonlinearities. The higher order terms actually cause the frequency multiplication.

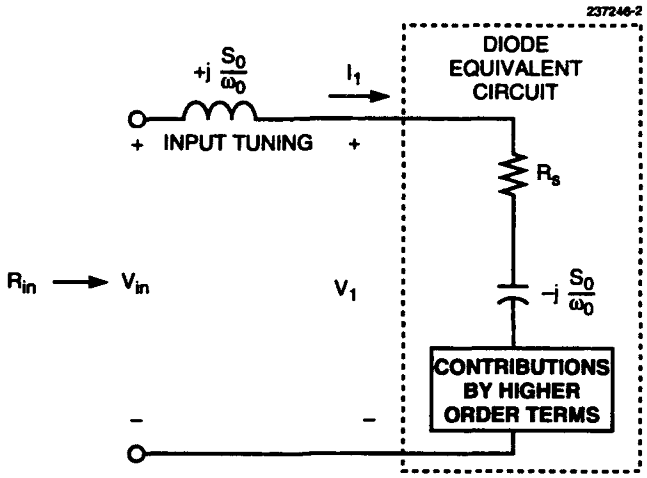

Figure 2. Input circuit.

To calculate the input impedance in terms of the normalized currents, elastances, and series resistances, the equations for the input resistance and the input voltage are needed from Figure 2:

$$R_{\text{in}} = \frac{V_{\text{in}}}{I_1} \quad \text{and} \tag{18}$$

$$V_{\text{in}} = j\frac{S_o}{\omega_o} I_1 + V_1 \quad . \tag{19}$$

Using Equations (18) and (19), the V_1 term of Equation (16) can be rewritten as:

$$R_{\text{in}} - j\frac{S_o}{\omega_o} = R_s - j\frac{1}{\omega_o} \sum_{l=-n}^{n} D_l S_{1-l} \tag{20}$$

because only the fundamental current is allowed to flow in this circuit. If identical terms on both sides of Equation (20) are eliminated, it reduces to:

$$R_{\text{in}} = -j\frac{1}{\omega_o}\left[\sum_{l=-n}^{0} D_l S_{1-l} + \sum_{l=2}^{n} D_l S_{1-l}\right] + R_s \quad . \tag{21}$$

Notice that the two summations are the same as one summation from $-n$ to n except for the S_o term at $l = 1$, which is a result of the input inductor tuning out the constant elastance.

The output circuit shown in Figure 3 can be treated in a similar manner. Again, there is an output inductor that tunes out the constant elastance at the output frequency. Here, the lower order terms create the frequency-multiplied signal. The equation for the nth harmonic voltage is also needed:

$$V_n = \left[-R_{\text{out}} - j\frac{S_o}{n\omega_o} \right] D_n I_1 \quad . \tag{22}$$

Using Equation (22), the V_n term of Equation (16) can be rewritten as

$$-R_{\text{out}} D_n - j\frac{S_o D_n}{n\omega_o} = R_s D_n - j\frac{1}{n\omega_o} \sum_{l=-n}^{n} D_l S_{n-l} \tag{23}$$

or, if identical terms on both sides are eliminated, as:

$$R_{\text{out}} = j\frac{1}{n\omega_o} \sum_{l=-n}^{n-1} \frac{D_l}{D_n} S_{n-l} - R_s \quad . \tag{24}$$

Again, notice that the constant elastance has been tuned out, and only the nth harmonic current is permitted to flow.

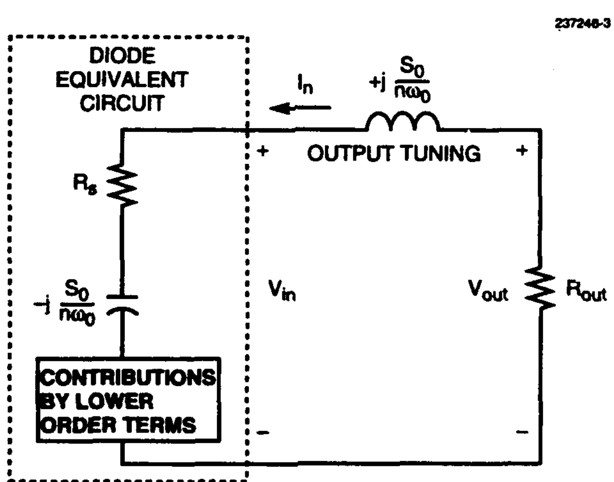

Figure 3. Output circuit.

Finally, the same procedure is performed for the idler circuits shown in Figure 4. As before, there is an inductor in each idler circuit to tune out the constant elastance at the idler frequency. However, there is no series resistance in the circuit other than the resistance of the diode. The expression for the harmonic voltage is

$$V_k = -j\frac{S_o}{k\omega_o}D_k I_1 \quad . \tag{25}$$

Using Equation (25), the V_k term of Equation (16) can be rewritten as:

$$-j\frac{S_o}{k\omega_o}D_k = R_s D_k - j\frac{1}{k\omega_o}\sum_{l=-n}^{N} D_l S_{k-l} \quad . \tag{26}$$

Again, after eliminating identical terms on both sides, Equation (26) reduces to:

$$0 = R_s D_k - j\frac{1}{D_k k\omega_o}\left[\sum_{l=-n}^{k-1} D_l S_{k-l} + \sum_{l=k+1}^{n} D_l S_{k-l}\right] \quad . \tag{27}$$

Again, notice that all the constant elastances have been tuned out of all the idler circuits, and only the *k*th harmonic current is permitted to flow.

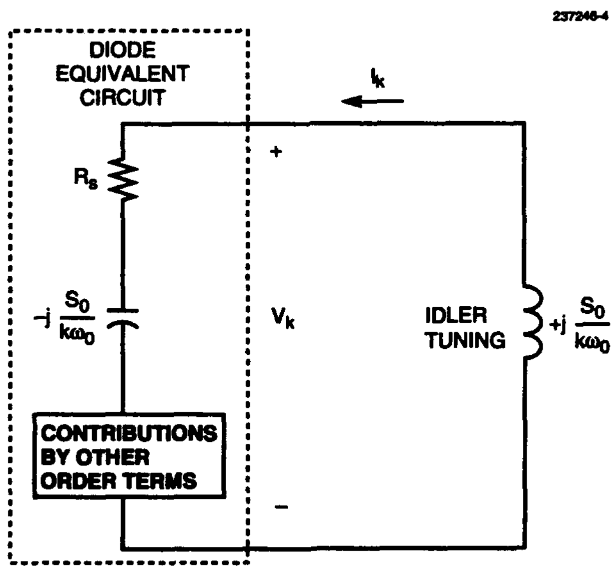

Figure 4. Idler circuits.

Because all the voltages, currents, and elastances are real, the bottom half of the matrix Equation (17) *can be elimin*ated, where $k < 0$. The equation for V_0 can also be ignored because a different method is used to design the bias circuit. In addition, because the bias currents are typically several orders of magnitude smaller than the other currents, they can be ignored. Therefore, a matrix equation can be written from Equations (21), (24), and (27) as:

$$\begin{bmatrix} R_{out} \\ 0 \\ \vdots \\ 0 \\ R_{in} \end{bmatrix} = R_s \begin{bmatrix} -1 \\ D_{n-1} \\ \vdots \\ D_2 \\ 1 \end{bmatrix} + \begin{bmatrix} 0\,, & & j\frac{1}{n\omega_o}\sum_{l=-n}^{n-1}\frac{D_l}{D_n}S_{n-l} \\ \cdot\,\cdot\,, & \cdot\,\cdot\,, & \cdot \\ -j\frac{1}{D_k k\omega_o}\sum_{l=-n}^{k-1} D_l S_{k-l}\,, & 0\,, & -j\frac{1}{D_k k\omega_o}\sum_{l=k+1}^{n} D_l S_{k-l} \\ \cdot\,\cdot\,, & \cdot\,\cdot\,, & \cdot \\ -\frac{j1}{\omega_o}\sum_{l=-n}^{0} D_l S_{1-l}\,, & 0\,, & -j\frac{1}{\omega}\sum_{l=2}^{n} D_l S_{1-l} \end{bmatrix} \times \begin{bmatrix} 1 \\ 1 \\ \vdots \\ 1 \\ 1 \end{bmatrix} \quad . \tag{28}$$

Equation (28), which is referred to later in this report, is the fundamental matrix equation for nonlinear reactive multipliers where only the first N currents are allowed to flow.

The important unknowns in Equation (28) are the elastance coefficients. To get these coefficients, the analysis must be constrained to deal with a certain type of nonlinear reactance. As mentioned earlier, the nonlinear reactance used here will be that of a punch-through varactor diode.

To make the mathematics easier, incremental elastance is used instead of incremental capacitance. Incremental or small signal elastance is defined as:

$$s(q) = \frac{1}{c(q)} = \frac{dv}{dq} \quad . \tag{29}$$

The incremental elastance for the punch-through varactor model is a step function (Figure 5) and is

$$s(q) = \begin{cases} S_{\max} & \text{for} \quad q > 0 \\ 0 & \text{for} \quad q \le 0 \end{cases} \quad . \tag{30}$$

The step function results when the punch-through diode is reverse-biased, and the depletion region rapidly expands to encompass the whole diode. Once that happens, adding any more charge does not change the diode's elastance. The punch-through diode's forward characteristic is a result of its extremely long minority carrier lifetime, τ. Because τ is much greater than the fundamental period, the extra charge in the depletion region never gets a chance to be swept away. Consequently, the diode appears to have infinite capacitance or zero elastance in the forward direction [3].

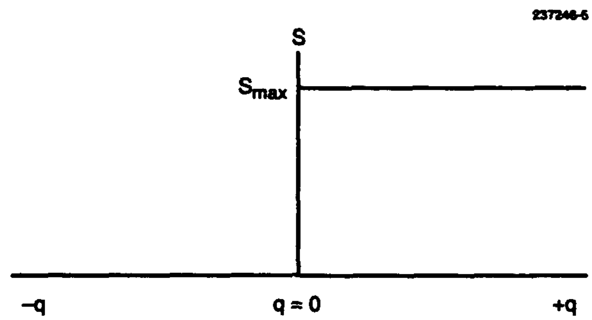

Figure 5. Elastance versus charge characteristic of punch-through diodes.

The only problem with Equation (30) is that it is a function of the charge q, and it should be a function of time for the matrix Equation (28). An expression for $q(t)$ is needed. Though $q(t)$ is yet unknown, it is assumed that it crosses the x-axis once every 180° at the fundamental frequency or

$$q(t)=\begin{cases}\leq 0 & \text{for} \quad (t_d+nT)-\dfrac{T}{4}<t<(t_d+nT)+\dfrac{T}{4} \\ >0 & \text{for} \quad (t_d+nT)+\dfrac{T}{4}\leq t\leq (t_d+nT)+\dfrac{3T}{4}\end{cases}, \tag{31}$$

where t_d is a time delay with respect to $t = 0$. Because the elastance versus charge relationship is a step function, this is enough information to determine $s(t)$. After determining the specific charge coefficients for doublers and triplers, this assumption will be validated. Therefore, using Equations (30) and (31), $s(t)$ can be calculated as:

$$s(t)=\begin{cases} 0 & \text{for} \quad (t_d+nT)-\dfrac{T}{4}<t<(t_d+nT)+\dfrac{T}{4} \\ S_{max} & \text{for} \quad (t_d+nT)+\dfrac{T}{4}\leq t\leq (t_d+nT)+\dfrac{3T}{4}\end{cases}. \tag{32}$$

The elastance waveform $s(t)$ is shown in Figure 6.

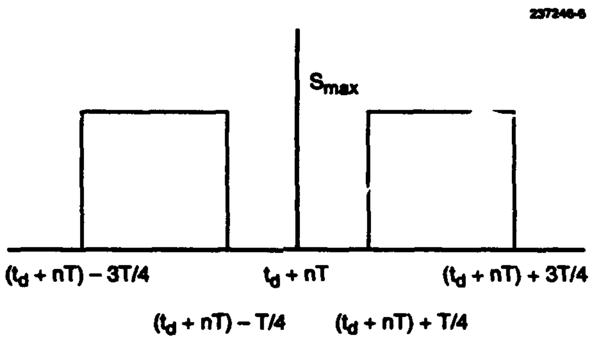

Figure 6. Elastance waveform for a punch-through varactor diode.

Now that the elastance function exists with respect to time, the elastance coefficients can be calculated by substituting Equation (32) into (9) with a result of:

$$S_k = \frac{1}{T} \int_{(t_d+nT)+\frac{T}{4}}^{(t_d+nT)+\frac{3T}{4}} S_{\max} e^{-jk\omega_o x} dx \quad . \tag{33}$$

After performing the integration, the result is

$$S_k = \frac{S_{\max}}{-jk\omega_o T} e^{-jk\omega_o (t_d+nT)} \left[e^{-jk\omega_o \frac{3T}{4}} - e^{-jk\omega_o \frac{T}{4}} \right] \quad . \tag{34}$$

Because $T = 2\pi/\omega_o$ and $e^{-j2\pi} = e^{-jn2\pi} = 1$, Equation (34) can be reduced to:

$$S_k = \frac{S_{\max}}{2} e^{-jk(\omega_o t_d + \pi)} \operatorname{sinc}\left(k \frac{\pi}{2} \right) \quad . \tag{35}$$

Let $\omega_o t_d = \theta$; then Equation (35) can be written as:

$$S_k = \frac{S_{max}}{2} e^{-jk(\theta+\pi)} \text{sinc}\left(k\frac{\pi}{2}\right) \quad , \tag{36}$$

or by substituting Equation (36) into the [A] matrix, Equation (14) can be expanded to:

$$A_{lk} = -j\frac{S_{max}}{2\omega_o k} \text{sinc}\left[(k-l)\frac{\pi}{2}\right] e^{-j(k-l)(\theta+\pi)} \quad . \tag{37}$$

Though the preceding model for the punch-through diodes produces good results, there are some differences between it and a real diode. Note that it was assumed that the transition between the forward and reverse characteristic occurs at zero charge, when in reality it occurs at a slightly negative charge. In addition, the transition is not a sharp step function, but rather it takes some positive charge before the elastance reaches S_{max}. Note that too, S_{max} is not completely flat, but rises slightly with increased positive charge. Besides differences between the model and reality, also keep in mind that charge waveforms other than those assumed may be more efficient.

The last variables that are still unknown in matrix Equation (28) are the current coefficients D_k. Because the first and last rows in Equation (28) determine the output and input resistances, the $n-2$ idler equations remain to determine the $n-1$ current coefficients. Therefore, to solve for the current coefficients, one more equation or constraint is added; that is, that the efficiency ϵ is at a maximum [8]. The efficiency is the ratio of the output power to the input power or

$$\varepsilon(D_2,\cdots,D_n) = \frac{P_{out}}{P_{in}} = \frac{\frac{1}{2}R_{out}(I_n + I_{-n})(I_n + I_{-n})^*}{\frac{1}{2}R_{in}(I_1 + I_{-1})(I_1 + I_{-1})^*} \quad , \tag{38}$$

which reduces to

$$\varepsilon(D_2,\cdots,D_n) = \frac{R_{out}(D_n + D_n{}^*)^2}{4R_{in}} \quad . \tag{39}$$

Next, the idler equations are used to reduce the efficiency to a function of only one of the current coefficients. Then the efficiency is differentiated with respect to the remaining current coefficients and set to zero as:

$$\frac{d\varepsilon(D_k)}{dD_k} = 0 \quad . \tag{40}$$

Finally, Equation (40) and the idler equations are used to calculate the remaining current coefficients. Because these equations are complicated, it is difficult to solve them for maximum efficiency in the general case. They will be solved later when specific order multipliers are examined.

Once the current coefficients are established, the charge coefficients must be calculated to determine whether the charge waveform violates the assumption that it crosses the x-axis once every 180° at the fundamental frequency. The charge waveform is the integral of the current waveform, so assuming zero initial charge, it is

$$q(t) = \int i(t)\, dt = \sum_{k=-n}^{n} \frac{I_1 D_k}{jk\omega_o} e^{jk\omega_o t} \quad . \tag{41}$$

Therefore, the charge coefficients are

$$Q_k = -j \frac{I_1 D_k}{k\omega_o} \quad . \tag{42}$$

Up to now, no limits were set as to how much input power to give the diode. However, real varactor diodes can only withstand a certain reverse voltage or charge before they break down. Because it is desirable to operate below the breakdown voltage V_B it is necessary to know the maximum input power. Start by determining the time at which the charge reaches its maximum [8], which occurs when the derivative of charge, i.e., current, is zero. Using Equation (4) and setting it equal to zero results in:

$$0 = \sum_{k=-n}^{n} D_k e^{jk\omega_o t_{qmax}} \quad . \tag{43}$$

Once again, this result is too complex to solve in the general case and will be solved when specific order multipliers are examined. From Equations (41) and (43), the maximum charge $Q_{\max}$ is

$$Q_{\max} = -j \frac{I_1}{\omega_o} \sum_{k=-n}^{n} \frac{D_k}{k} e^{jk\omega_o t_{qmax}} \quad . \tag{44}$$

Integrating Equation (29), the elastance charge relationship, results in the voltage charge relationship:

$$v = \int s(q)dq \quad , \tag{45}$$

which for punch-through diodes, when $q > 0$, is

$$V_{\max} = S_{\max} Q_{\max} \quad . \tag{46}$$

Substituting Equation (44) into (46) and solving for I_1^2, results in :

$$I_1^2 = \frac{V_{\max}^2 \omega_o^2}{S_{\max}^2 \left| \sum_{k=-n}^{n} \frac{D_k}{k} e^{jk\omega_o t_{q\max}} \right|^2} \quad . \tag{47}$$

Because the input power is

$$P_{\text{input}} = 2R_{\text{input}} I_1^2 \quad , \tag{48}$$

where the factor of 2 is due to the two currents I_1 and I_{-1}, the maximum input power is

$$P_{\text{in}} = \frac{2V_{\max}^2 R_{\text{in}} \omega_o^2}{S_{\max}^2 \left| \sum_{k=-n}^{n} \frac{D_k}{k} e^{jk\omega_o t_{q\max}} \right|^2} \quad . \tag{49}$$

A complete, generalized, mathematical description of a punch-through varactor diode multiplier has been written.

2.1 THE DOUBLER

The two most practical multipliers to build are the doubler and the tripler. The general design parameters for the doubler will be calculated next, beginning with the matrix Equation (28), which reduces to the two scalar equations

$$R_{\text{out}} = -R_s + j\frac{1}{2\omega_o D_2}\left[S_1 + S_3 + D_2^* S_4\right] \quad \text{and} \tag{50}$$

$$R_{\text{in}} = R_s - j\frac{1}{\omega_o}\left[S_1^* D_2 + S_2 + D_2^* S_3\right] \quad . \tag{51}$$

Using the elastance coefficients determined by Equation (36), (50) and (51) reduce to

$$R_{\text{out}} = -R_s + j\frac{S_{\max}}{4\omega_o D_2}\left[0.6366 e^{-j(\theta+\pi)} - 0.2122 e^{-j3(\theta+\pi)}\right] \quad \text{and} \tag{52}$$

$$R_{in} = R_s - j\frac{S_{max}}{2\omega_o}\left[0.6366e^{j(\theta+\pi)}D_2 - 0.2122e^{-j3(\theta+\pi)}D_2^*\right] \quad . \tag{53}$$

For the doubler to work properly, both the input and output impedances must be positive and real. This criterion limits the combinations of θ and $<D_2$ that are valid but does not uniquely determine either. For simplicity, let $\theta = -90°$ and $< D_2 = 0°$. Consequently, Equations (52) and (53) reduce to:

$$R_{out} = -R_s + 0.8488\frac{S_{max}}{4\omega_o D_2} \quad \text{and} \tag{54}$$

$$R_{in} = R_s + 0.4244\frac{S_{max}D_2}{2\omega_o} \quad , \tag{55}$$

which are the general doubler equations for the output and input resistance.

Before using Equations (54) and (55), the current coefficient is calculated by maximizing the efficiency using Equation (39), which for the doubler reduces to:

$$\varepsilon(D_2) = \frac{0.8488S_{max}D_2 - 4R_sD_2^2\omega_o}{0.8488S_{max}D_2 + 4R_s\omega_o} \quad . \tag{56}$$

Differentiating Equation (56) with respect to D_2 and setting it equal to zero gives a quadratic equation. Using the quadratic formula, D_2 is

$$D_2 = -4.713\frac{R_s\omega_o}{S_{max}} + \sqrt{\frac{22.21R_s^2\omega_o^2}{S_{max}^2} + 1} \quad , \tag{57}$$

which reduces to

$$D_2 = 1 \tag{58}$$

for the lossless case. Knowing D_2 for the lossless case, R_{out} and R_{in} were calculated for the lossless case as

$$R_{out} = 0.4244\frac{S_{max}}{2\omega_o} \quad , \tag{59}$$

$$R_{in} = 0.2122 \frac{S_{max}}{\omega_o} \quad . \tag{60}$$

To determine if the assumption about the charge waveform is correct, the current, charge, and elastance waveforms are plotted for the lossless case. The charge coefficients from Equation (42) are

$$\frac{Q_1}{I_1} = -j\frac{1}{\omega_o} \quad \text{and} \quad \frac{Q_2}{I_1} = -j\frac{1}{2\omega_o} \quad . \tag{61}$$

As can be seen in Figure 7, the assumption proves true.

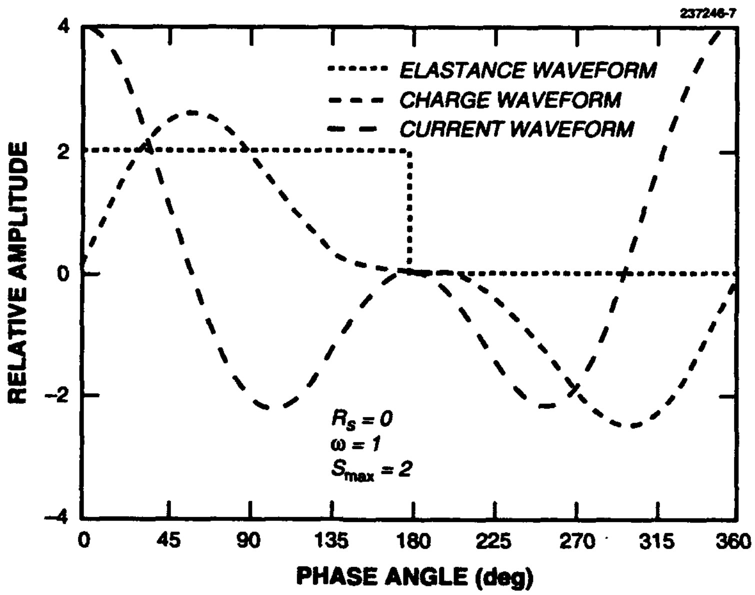

Figure 7. Current, charge, and elastance waveforms for a lossless doubler.

Next, an expression must be found for the maximum input power that a doubler can handle. First, find when maximum charge occurs, which is at zero current. Using the equation for the current in the case of the doubler, Equation (43), and after rearranging the exponential terms, results in:

$$\cos(\omega_o t_{q\,\max}) = -D_2 \cos(2\omega_o t_{q\,\max}) \quad , \tag{62}$$

which is an implicit expression that generally has to be solved numerically or graphically. However, for the lossless case the principle value of $t_{q\max}$ is

$$t_{q\max} = \frac{\pi}{3\omega_o} \quad \text{or} \quad 60^\circ \quad \text{at} \quad \omega_o \quad . \tag{63}$$

From Equation (49), the maximum input power for a doubler is

$$P_{in} = \frac{2V_{\max}^2\omega_o^2\left[R_s + \dfrac{0.2122 S_{\max} D_2}{\omega_o}\right]}{S_{\max}^2\left[2\sin(\omega_o t_{q\max}) + D_2\sin(2\omega_o t_{q\max})\right]^2} \quad . \tag{64}$$

For the lossless case, this reduces to:

$$P_{in} = 0.06287\frac{V_{\max}^2\omega_o}{S_{\max}} \quad . \tag{65}$$

These and all the other pertinent design equations for the doubler are listed in Appendix A for the general and the lossless cases.

2.2 THE TRIPLER

The tripler is a little more complicated than the doubler as it uses an idler circuit. The matrix Equation (28) for the tripler reduces to

$$R_{out} = -R_s + j\frac{1}{3\omega_o D_3}\left[D_3^* S_6 + D_2^* S_5 + S_4 + S_2 + D_2 S_1\right] \quad , \tag{66}$$

$$0 = R_s D_2 - j\frac{1}{2\omega_o}\left[D_3^* S_5 + D_2^* S_4 + S_3 + S_1 + D_3 S_1^*\right] \quad \text{, and} \tag{67}$$

$$R_{in} = R_s - j\frac{1}{\omega_o}\left[D_3^* S_4 + D_2^* S_3 + S_2 + D_2 S_1^* + D_3 S_2^*\right] \quad . \tag{68}$$

Using the elastance coefficients determined by Equation (36), (66) through (68) reduce to:

$$R_{out} = -R_s + j\frac{S_{\max}}{6\omega_o D_3}\left[0.1273 e^{-j5(\theta+\pi)} D_2^* + 0.6366 e^{-j(\theta+\pi)} D_2\right] \quad , \tag{69}$$

$$0 = R_s D_2 - j\frac{S_{\max}}{4\omega_o}$$
$$\left[0.1273e^{-j5(\theta+\pi)}D_3^* - 0.2122e^{-j3(\theta+\pi)} + 0.6366(e^{-j(\theta+\pi)} + e^{-j(\theta+\pi)}D_3)\right] \quad , \tag{70}$$

and

$$R_{\text{in}} = R_s - j\frac{S_{\max}}{2\omega_o}\left[-0.2122e^{-j3(\theta+\pi)}D_2^* + 0.6366e^{j(\theta+\pi)}D_2\right] \quad . \tag{71}$$

As in the doubler, the input and output impedances must be positive and real. This criterion limits the combinations of $\Theta < D_2$, and $< D_3$ that are valid but does not uniquely determine any. For simplicity, let $\Theta = -90°$ and $< D_2 = < D_3 = 0°$, reducing Equations (69) through (71) to:

$$R_{\text{out}} = -R_s + \frac{S_{\max}}{6\omega_o D_3}[0.7639D_2] \quad , \tag{72}$$

$$0 = R_s + \frac{S_{\max}}{4\omega_o D_2}[0.5093D_3 - 0.8488] \quad \text{, and} \tag{73}$$

$$R_{\text{in}} = R_s + \frac{S_{\max}}{2\omega_o}[0.4244D_2] \quad , \tag{74}$$

which are the general tripler equations for the output resistance, idlers, and input resistance.

Before using Equations (72) through (74), the current coefficients must be determined. Use the idler Equation (27) to get D_3 in terms of D_2 or:

$$D_3 = 1.667 - \frac{7.854\omega_o D_2 R_s}{S_{\max}} \quad , \tag{75}$$

which for the lossless case reduces to:

$$D_3 = 1.667 \quad . \tag{76}$$

Then, to determine D_2, use the efficiency Equation (39) to get:

$$\varepsilon(D_2, D_3) = \frac{R_{\text{out}}(2D_3)^2}{4R_{\text{in}}} \quad . \tag{77}$$

After making all the required substitutions, Equation (77) is

$$\varepsilon(D_2, D_3) = \frac{0.1273S_{\max}D_2D_3 - R_sD_3^2\omega_o}{0.2122S_{\max}D_2 - R_s\omega_o} \quad . \tag{78}$$

To determine D_2, substitute Equation (75) into (78) and differentiate it with respect to D_2. Because the maximum efficiency is desired, solve the derivative equal to zero to get:

$$D_2 = -4.713\frac{R_s\omega_o}{S_{\max}} \pm \sqrt{83.92\frac{R_s^2\omega_o^2}{S_{\max}^2} - 26.19\frac{R_s\omega_o}{S_{\max}} + 3.781} \quad , \tag{79}$$

which reduces to:

$$D_2 = 1.944 \tag{80}$$

for the lossless case. Knowing D_2 and D_3, R_{out} and R_{in} are calculated for the lossless case as:

$$R_{\text{out}} = 0.4454\frac{S_{\max}}{3\omega_o} \quad \text{and} \tag{81}$$

$$R_{\text{in}} = 0.4125\frac{S_{\max}}{\omega_o} \quad . \tag{82}$$

Before proceeding further, the assumption that the charge waveform crosses the x-axis once every 180° at the fundamental frequency needs to be checked. The charge coefficients from Equation (42) are

$$\frac{Q_2}{I_1} = -j\frac{0.9720}{\omega_o} \quad \text{and} \quad \frac{Q_3}{I_1} = -j\frac{0.5557}{\omega_o} \quad . \tag{83}$$

By plotting the charge, current, and elastance waveforms in Figure 8, the assumption holds true a second time.

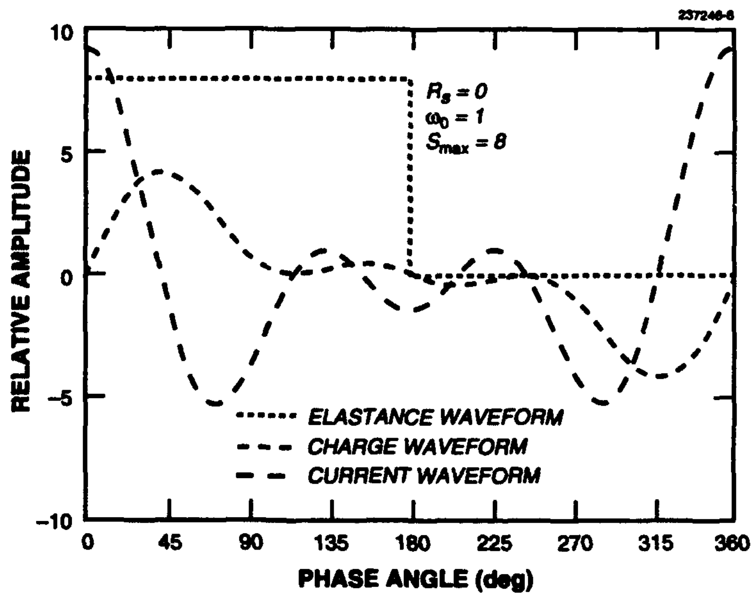

Figure 8. Current, charge, and elastance waveforms for a lossless tripler.

Next, the maximum input power that the diode can withstand must be determined. As in the doubler, first determine the time of maximum charge from Equation (43) as:

$$0 = \cos(\omega_o t_{q\,\max}) + D_2 \cos(2\omega_o t_{q\,\max}) + D_3 \cos(3\omega_o t_{q\,\max}) \quad . \tag{84}$$

For the lossless case, the easiest way to solve Equation (84) for $t_{q\max}$ is graphically, from which is obtained:

$$t_{q\,\max} = \frac{0.7295}{\omega_o} \quad \text{or} \quad 41.80^\circ \quad \text{at} \quad \omega_o \quad . \tag{85}$$

Knowing $t_{q\max}$, the maximum input power is calculated from Equation (49) as:

$$P_{\text{in}} = \frac{2V_{\max}^2 \omega_o^2 R_s + 0.4244 V_{\max}^2 \omega_o D_2 S_{\max}}{S_{\max}^2 \left[\frac{2}{3} D_3 \sin(3\omega_o t_{q\,\max}) + D_2 \sin(2\omega_o t_{q\,\max}) + 2\sin(\omega_o t_{q\,\max})\right]^2} \quad . \tag{86}$$

And finally, for the lossless case Equation (86) reduces to:

$$P_{\text{in}} = 0.04742 \frac{V_{\max}^2 \omega_o}{S_{\max}} \quad . \tag{87}$$

These and all other pertinent design equations for the tripler are listed in Appendix B for both the general and the lossless cases.

3. DESIGN PROCEDURE

3.1 THE DOUBLER

The doubler circuit is the simplest multiplier, and it is shown in Figure 9. The output trap is tuned to the fundamental frequency and prevents it from escaping through the output port. The input trap is likewise tuned to the second harmonic to prevent it from leaking back to the source. In addition, the input trap is inductive at the input frequency and tunes out the average elastance of the varactor in the input circuit. However, a separate tuning inductor is needed on the output side to tune out the average elastance of the varactor because the output trap is capacitive.

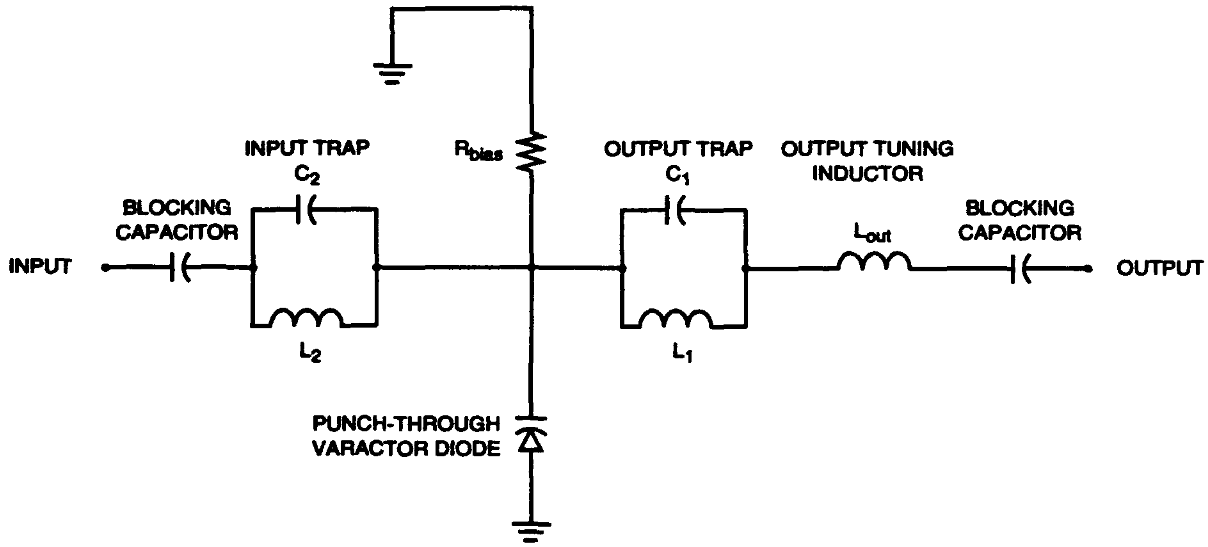

Figure 9. Punch-through varactor diode doubler circuit.

Generally, when designing varactor multipliers, the relationship

$$R_s \omega_o << S_{max} \tag{88}$$

is valid where R_s is the series resistance of the diode, ω_o is the input frequency of the multiplier, and S_{max} is the maximum elastance of the diode when it is reversed biased. Note that the elastance is the reciprocal of capacitance. With this assumption a doubler can be designed using the lossless column of the generic doubler equations at the beginning of Appendix A.

In a punch-through varactor doubler, the input and output resistances are the same. Therefore, S_{max} or C_{min} is determined by the characteristic impedance of the system Z_o in which the doubler will be used. Using the equation for either the input or output resistance in Appendix A, the capacitance at the diode's breakdown voltage is calculated as:

$$C_{\min} = 0.03377 \frac{1}{Z_o f_o} \quad , \tag{89}$$

where f_o is the input frequency in Hertz. Next, the minimum required breakdown voltage is calculated from the expected maximum input power using the input power expression in Appendix A, resulting in

$$V_{\max} = 1.591 \sqrt{\frac{P_{\text{in}}}{\mathrm{f_o} C_{\min}}} \quad . \tag{90}$$

There should be enough input power to get the maximum voltage above 5 V, otherwise the diode operates more like an abrupt junction varactor diode, and the preceding equations are not valid.

The bias resistor is calculated from

$$R_{\text{bias}} = \frac{\tau}{C_{\min}} \quad , \tag{91}$$

where τ is the minority carrier lifetime of the diode [9]. This expression is approximate, so the actual value of R_{bias} should be determined experimentally. Finally, τ must be much longer than the period of the fundamental frequency for reasons given previously.

For the input trap to be resonant at the output frequency and tune out the average elastance of the varactor diode at the input frequency, C_2 and L_2 must be

$$C_2 = \frac{2}{3} C_{\min} \quad \text{and} \tag{92}$$

$$L_2 = \frac{1}{4\omega_o^2 C_2} \quad . \tag{93}$$

The output circuit, unlike the input circuit, is not uniquely determined by the varactor because of the extra tuning inductance. To get unique values, let the reactance of the output trap equal the average reactance of the varactor at the output frequency. Using this constraint, the output circuit values are

$$C_1 = \frac{8}{3} C_{\min} \quad , \tag{94}$$

$$L_1 = \frac{1}{\omega_o^2 C_1} \quad \text{, and} \tag{95}$$

$$L_{out} = \frac{2}{3} L_1 \quad . \tag{96}$$

All the doubler circuit design equations appear in Appendix A.

3.2 THE TRIPLER

The tripler is more complicated than the doubler due to the addition of idlers at the second harmonic. The complete tripler circuit is shown in Figure 10. Instead of one diode, the tripler shown here uses a matched pair of diodes, although a single diode tripler could also be used. Each diode in combination with its idler inductor L_2 resonates at the second harmonic, forming two series idlers. This arrangement constrains the second harmonic current to stay in the low impedance path of the two idlers. Also, operating the two diodes in push-pull mode considerably reduces all even-order harmonics at both the input and output, which is not possible with a single diode tripler.

The input and output traps work similarly to the doubler. The input trap prevents the third harmonic output signal from leaking into the input. It also tunes out the series reactance of L_2 and the diodes at the input frequency. Likewise, the output trap prevents the fundamental from leaking to the output port. Unlike the doubler, the output trap is also able to tune out the diode reactance because the needed inductor is already there as L_2.

Due to the additional complexity of the tripler, it is prone to instabilities from reactive out-of-band terminations. To prevent instabilities, bridge-tee circuits have been added in both the input and output sides. These circuits act like a through line at their designed frequency, while providing a known resistive termination to out-of-band frequencies [10].

The matching networks are simple L-networks. Because triplers are narrowband circuits, there is generally no need to use fancier matching networks.

Another cause of instabilities is an improperly designed bias circuit. The closer the bias resistor is to the diode, the less likely are instabilities [8]. In Figure 10, the bias resistors are connected directly across the diodes with no other intervening components.

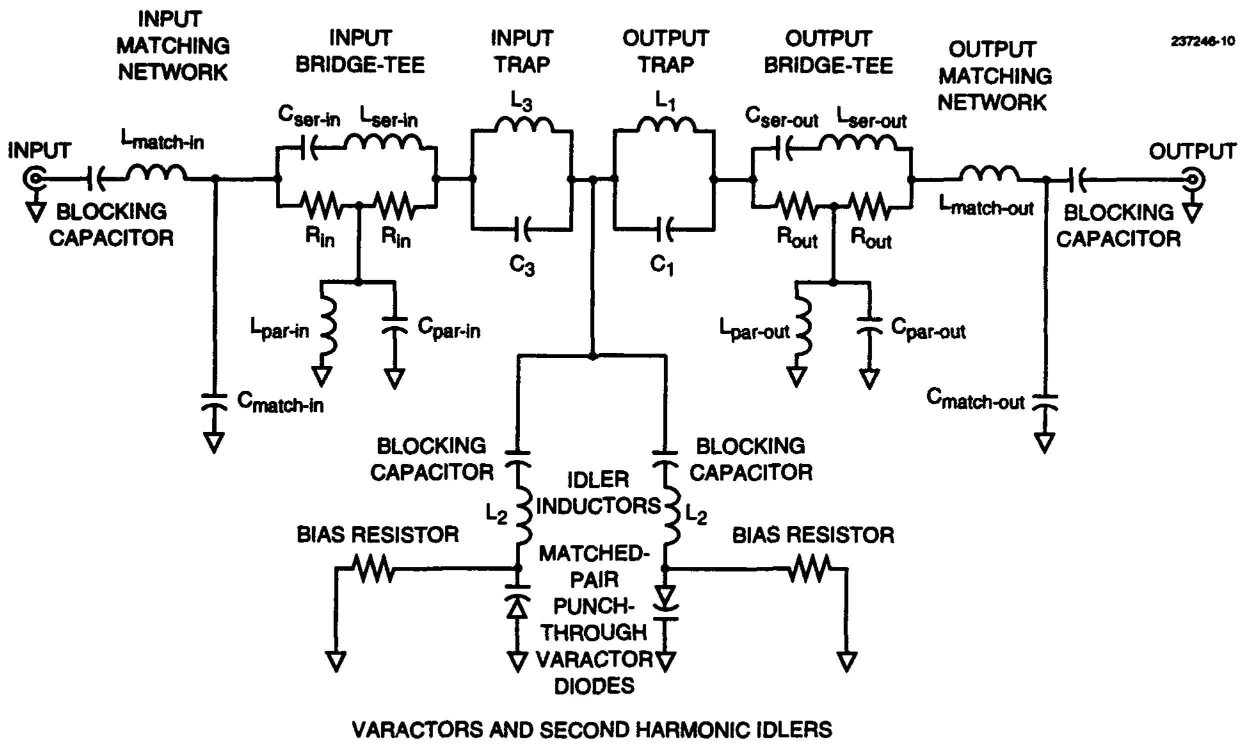

Figure 10. Punch-through varactor diode tripler circuit.

To calculate the component values, assume (as in the doubler) that the expression

$$R_s \omega_o << S_{\max} \tag{97}$$

holds true. This permits the use of the lossless column of the generic tripler equations in Appendix B. Unlike the doubler, the tripler's input and output impedances are not the same. To keep the components as realizable as possible, let the input and output resistances be determined by:

$$R_{\text{in}} = \frac{5}{3} Z_o \quad \text{and} \quad R_{\text{out}} = \frac{3}{5} Z_o \quad . \tag{98}$$

Note that R_{in} and R_{out} in Equation (98) are the circuit input and output resistances. Because of the two diodes that are effectively in parallel, the resistances in Equation (98) are one-half of those found in the beginning of Appendix B. Knowing the input resistance, the minimum reversed biased capacitance is

$$C_{\min} = 0.03283 \frac{1}{f_o R_{\text{in}}} \quad . \tag{99}$$

The idler inductors L_2 are then calculated as:

$$L_2 = \frac{1}{8\omega_o^2 C_{\min}} \quad . \tag{100}$$

As in the doubler, the breakdown voltage must be large enough to handle the expected input power. The required breakdown voltage is determined by using the formula for the input power in Appendix B, while keeping in mind that the voltage splits in half across the two diodes. Therefore, the breakdown voltage is

$$V_{\max} = 0.916 \sqrt{\frac{P_{\text{in}}}{f_o C_{\min}}} \quad . \tag{101}$$

The breakdown voltage required by the input power should be greater than 5 V or the tripler will not work properly. Generally, the greater the input power, the more efficient the multiplier. If the input power is too low, the diode will act more like an abrupt junction varactor rather than a punch-through varactor and will require a different set of design equations than those being used.

The bias resistors are calculated from

$$R_{\text{bias}} = \frac{\tau}{C_{\min}} \quad , \tag{102}$$

where τ is the minority carrier lifetime of the diode [9]. This expression is approximate, so the actual values of R_{bias} should be determined experimentally. Because even a pair of matched diodes is never absolutely identical, the two bias resistors will not necessarily be the same. Finally, τ must be much longer than the period of the fundamental frequency for reasons given earlier.

Before designing the bridge-tee circuits, the Q for each is determined. Generally, the higher the Q, the more stable the multiplier. On the other hand, the lower the Q, the more realizable the components. The exact Q depends on the quality of the available inductors and capacitors. For a given Q_{in}, the input bridge-tee values are

$$L_{\text{ser-in}} = \frac{R_{\text{in}} Q_{\text{in}}}{\omega_o} \quad , \qquad C_{\text{ser-in}} = \frac{1}{\omega_o R_{\text{in}} Q_{\text{in}}} \quad , \tag{103}$$

$$L_{\text{par-in}} = \frac{R_{\text{in}}}{Q_{\text{in}}\omega_{\text{o}}} \,, \quad \text{and} \qquad C_{\text{par-in}} = \frac{Q_{\text{in}}}{\omega_{\text{o}} R_{\text{in}}} \quad . \tag{104}$$

Likewise, the components values for the output bridge-tee are

$$L_{\text{ser-out}} = \frac{R_{\text{out}} Q_{\text{out}}}{3\omega_{\text{o}}} \quad , \qquad C_{\text{ser-out}} = \frac{1}{3\omega_{\text{o}} R_{\text{out}} Q_{\text{out}}} \quad , \tag{105}$$

$$L_{\text{par-out}} = \frac{R_{\text{out}}}{Q_{\text{out}} 3\omega_{\text{o}}} \,, \quad \text{and} \qquad C_{\text{par-out}} = \frac{Q_{\text{out}}}{3\omega_{\text{o}} R_{\text{out}}} \quad , \tag{106}$$

where R_{in} and R_{out} are the input and output resistances, respectively, of the tripler circuit.

Continuing with the remainder of the circuit, the input and output traps are calculated as [11]:

$$L_3 = \frac{4}{3} L_2 \quad , \qquad C_3 = \frac{2}{3} C_{\text{min}} \quad , \tag{107}$$

$$L_1 = \frac{20}{9} L_2 \quad , \quad \text{and} \quad C_1 = \frac{18}{5} C_{\text{min}} \quad . \tag{108}$$

Finally, the input and output matching networks are calculated as [12]:

$$L_{\text{match-in}} = \frac{Z_o}{\omega_o} \sqrt{\frac{R_{\text{in}}}{Z_o} - 1} \quad , \qquad C_{\text{match-in}} = \frac{\sqrt{\frac{R_{\text{in}}}{Z_o} - 1}}{\omega_o R_{\text{in}}} \quad , \tag{109}$$

$$L_{\text{match-out}} = \frac{R_{\text{out}}}{3\omega_o} \sqrt{\frac{Z_o}{R_{\text{out}}} - 1} \quad , \quad \text{and} \qquad C_{\text{match-out}} = \frac{\sqrt{\frac{Z_o}{R_{\text{out}}} - 1}}{3\omega_o Z_o} \quad . \tag{110}$$

A complete listing of the tripler circuit design equations appears in Appendix B.

4. DESIGN EXAMPLES

4.1 2.64-GHz DOUBLER

An example of a punch-through varactor doubler that was built at 2.64 GHz is shown in Figures 11 and 12. The circuit in Figure 12 also includes a single-stage amplifier before the doubler that is not shown in Figure 11. The doubler is designed for a 50-Ω system, so using Equation (89), C_{min} is calculated to equal 0.256 pF. Because an input power of 10 dBm is needed, Equation (90) is used to get a breakdown voltage of V_{max} = 6.12 V. The closest punch-through varactor diode that meets this voltage is a M/A COM MA44621A-C with a C_{min} = 0.25 pF and a V_{max} = 20 V. The series resistance is less than 5 Ω and because $R_s\omega_o = 8.29 \times 10^{10}$ is less than $S_{max} = 4 \times 10^{15}$, the lossless equations in Appendix A can be used safely. The calculated bias resistor using Equation (91) is R_{bias} = 40 KΩ. After experimenting with the bias resistor value, an optimum value of 44 KΩ was achieved.

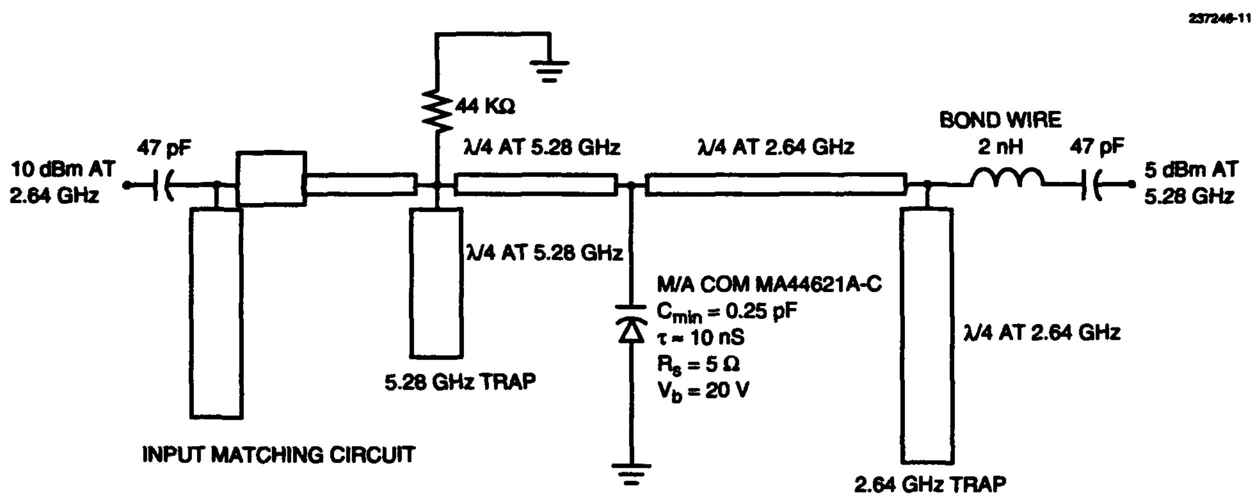

Figure 11. Schematic diagram of a 2.64-GHz punch-through varactor diode doubler.

Because of the high frequency involved, both the traps and the input matching circuit were implemented as microstrip transmission lines instead of lumped elements. The traps were implemented as two quarter-wavelength transmission lines in an "L" configuration. Though the input trap could have designed with the proper transmission line impedances to resonate with the average elastance of the diode as in the lumped element case, instead impedances were used that were realizable in microstrip. This decision required an extra L-matching network at the input and an ~2 nH inductor made of bond wires at the output. The L-matching network was determined by using a microwave CAD program and by experimentation.

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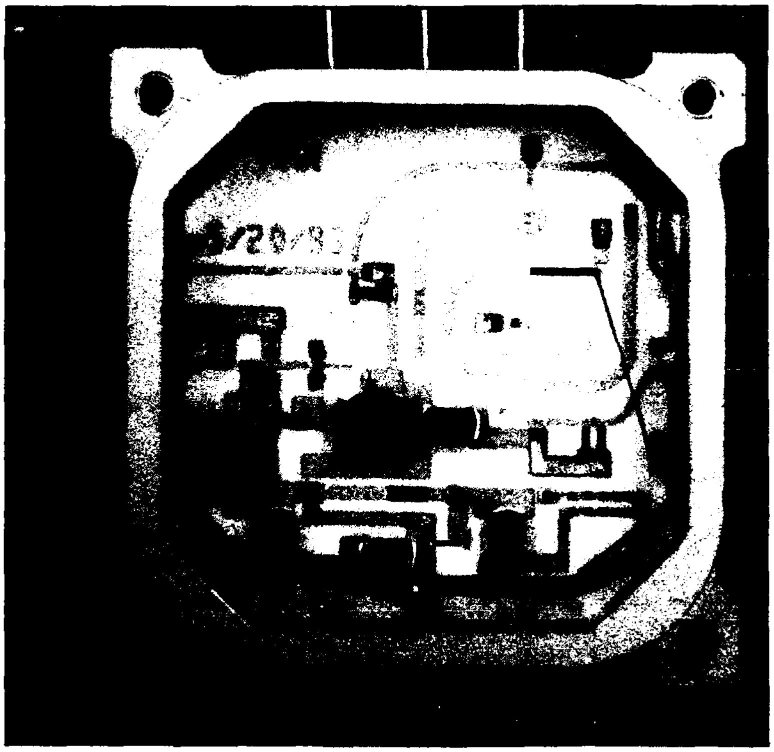

Figure 12. A 2.64-GHz punch-through varactor diode doubler as built.

Despite the high frequency and low input power, the multiplier performed well. With an input power of +8.93 dBm, it had an efficiency of 32%. Much of the loss was likely due to the microstrip lines in the circuit and in the test fixture used to test the packaged circuit. The input impedance and reflection coefficient are shown in Figure 13, and the relative output spectrum is shown in Figure 14.

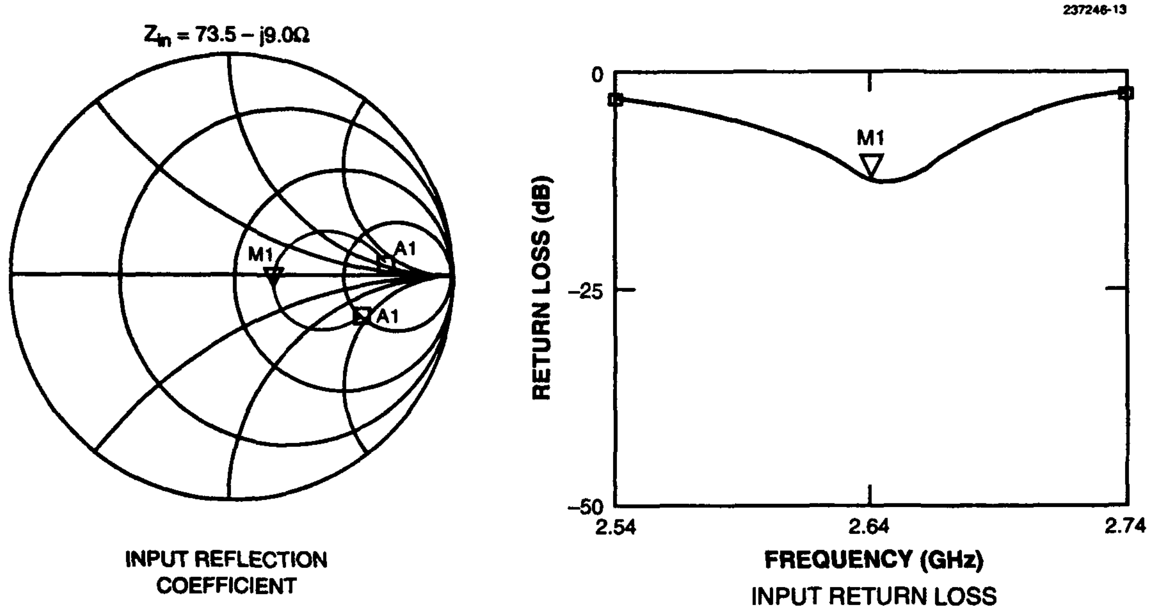

Figure 13. Input impedance and reflection coefficient of a 2.64-GHz punch-through varactor diode doubler.

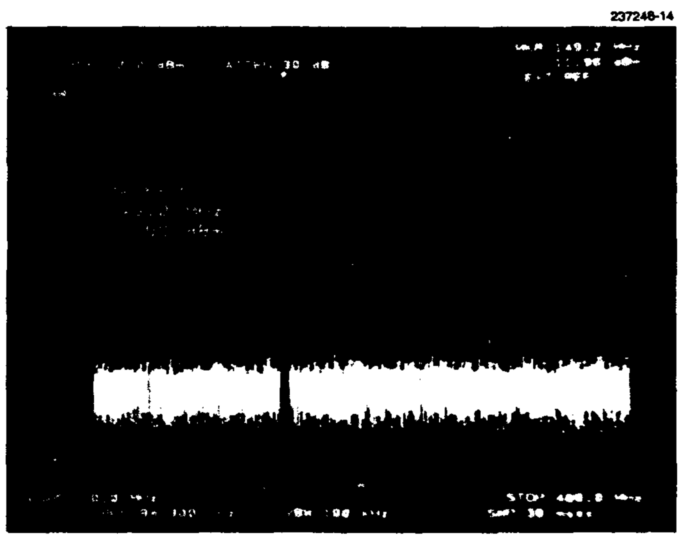

Figure 14. Output spectrum of a 2.64-GHz punch-through varactor diode doubler.

4.2 50-MHz TRIPLER

A 50-MHz tripler (shown in Figures 15 and 16) was built to test the tripler equations. It was designed for a 50-Ω system with 1 W of input power. From Equation (98) it is seen that R_{in} = 83 Ω and R_{out} = 30 Ω; Equation (99) indicates a need for C_{min} = 7.8 pF. The diode with the closest specifications is an Alpha Industries DVB6145-19 with a C_{min} = 8.8 pF, V_B = 75 V, R_s ~5 Ω, and τ ~240 nS. From the diode specifications, it is obvious that $R_s \omega_o = 3.142 \times 10^9$ is much less than $S_{max} = 1.136 \times 10^{11}$, so the lossless equations in Appendix B can be used. Therefore, using Equations (81) and (82), the input and output resistances for the DVB6145-19 are R_{in} = 74.6 Ω and R_{out} = 26.8 Ω. Using Equation (101), V_{max} = 43.7 V for 1 W of input power, leaving a good margin.

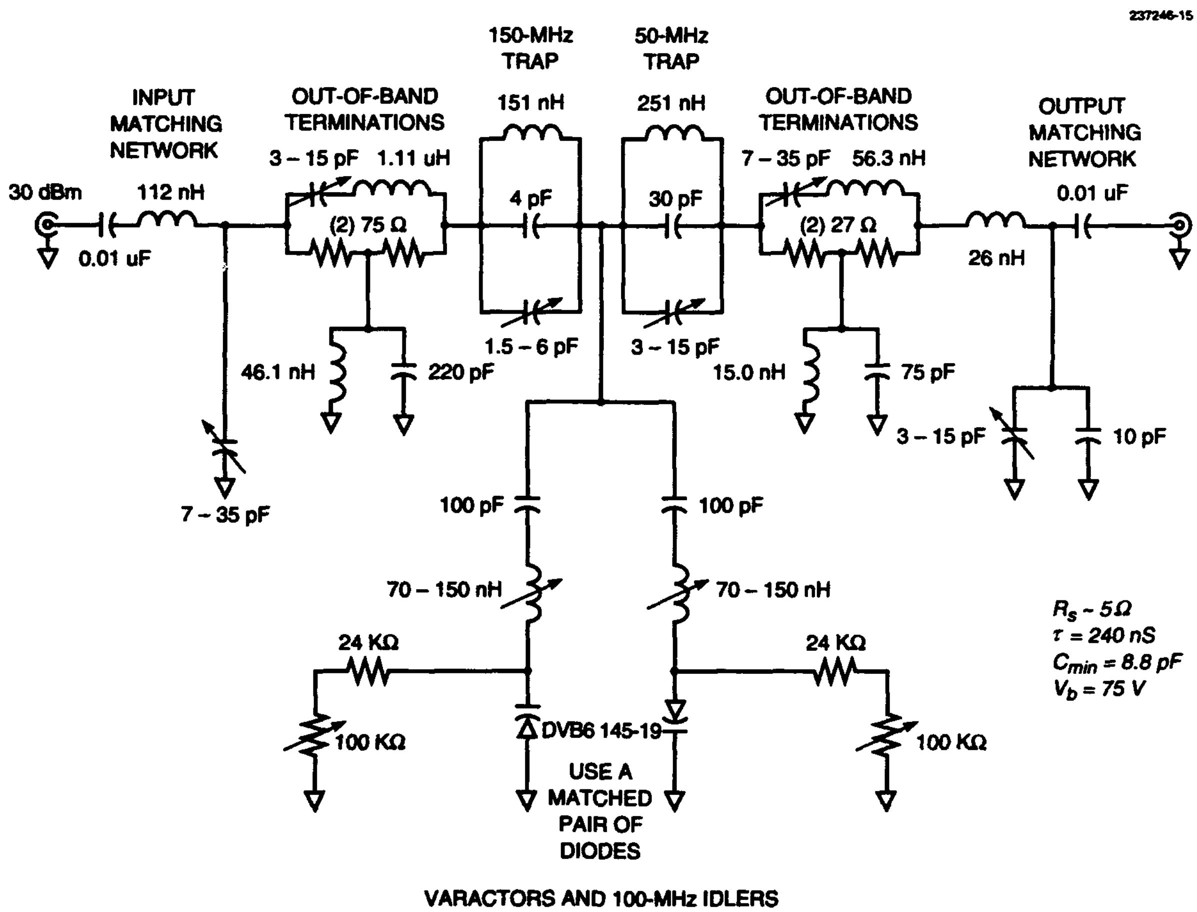

Figure 15. Schematic diagram of a 50-MHz punch-through varactor diode tripler.

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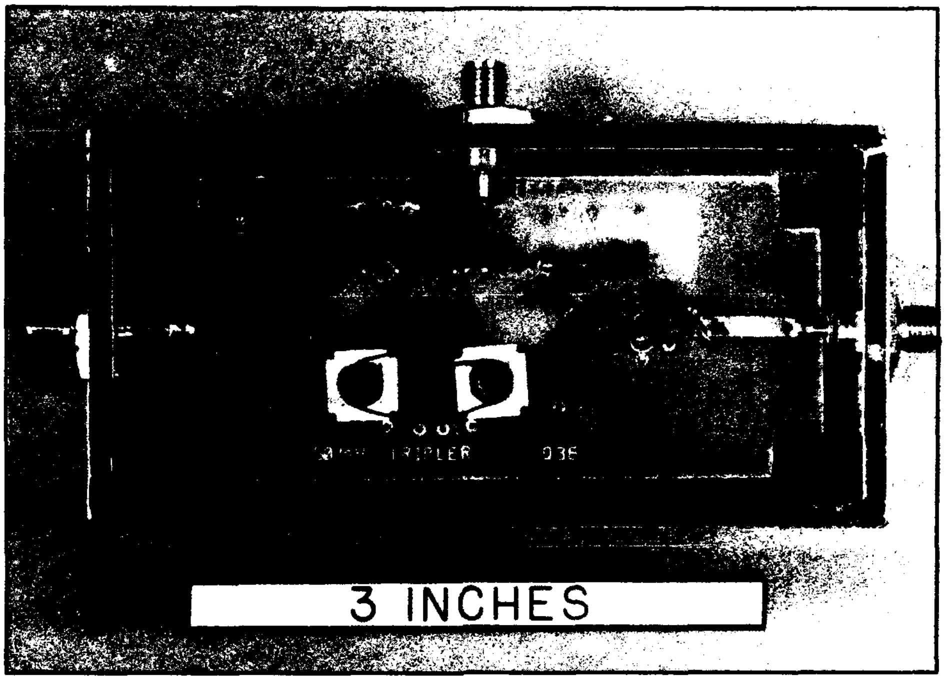

Figure 16. The 50-MHz punch-through varactor diode tripler as built.

The idlers also include the idler inductance and the bias resistor. The idler inductor is determined from Equation (100) to be 143.9 nH, and the bias resistor is calculated from Equation (102) to be 27.3 KΩ.

For the bridge-tees, an input Q of 5 and an output Q of 2 worked well and gave realizable component values. The values for the components were calculated from Equations (103) through (106) and are shown in Figure 15.

The component values for the two traps are calculated from Equations (107) and (108). However, the average elastance of the diode is more like 2.2 $C_{min,}$ so both the idler inductors and the trap components are altered slightly from the requirements of Equations (103) through (108).

Finally, the input and output matching section components are calculated from Equations (109) and (110). Because of the large number of reactive components that need to be properly adjusted, many of the components were implemented as variable capacitors or inductors.

Because its operating frequency is much lower, the tripler is more efficient than the doubler. Even though the tripler was tested with only +15 dBm of input power to make it easier to characterize, it had an efficiency of 53%. The input impedance and reflection coefficient are shown in Figure 17, and the output spectrum is shown in Figure 18.

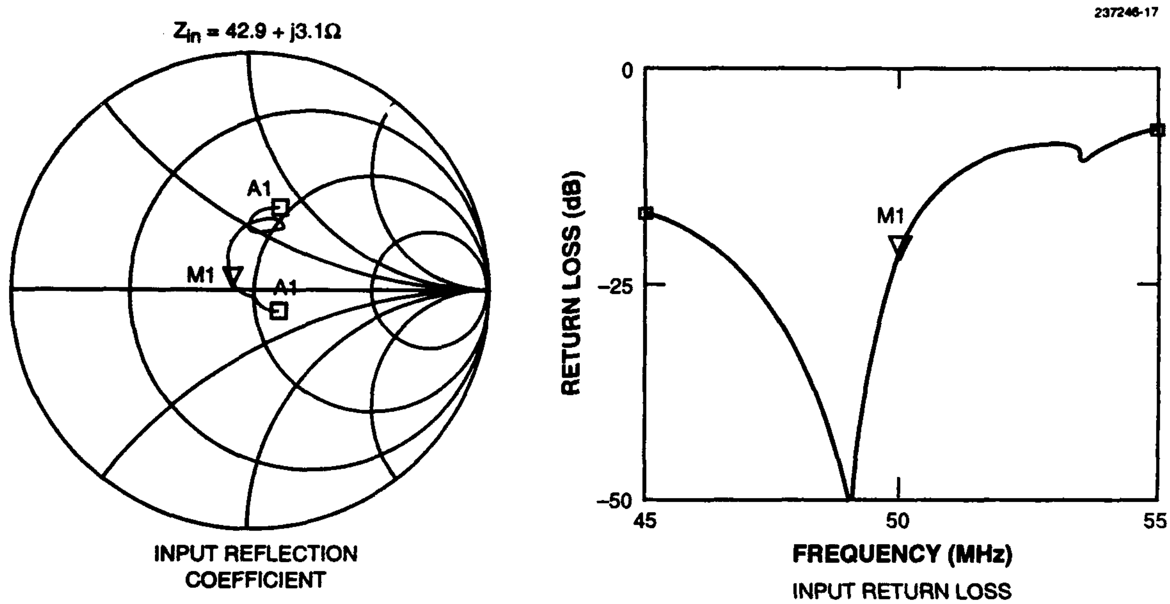

Figure 17. Input impedance and reflection coefficient of the 50-MHz punch-through varactor diode tripler.

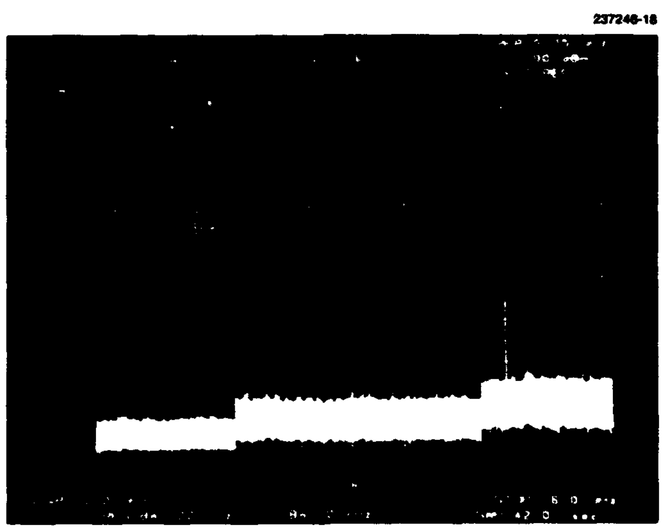

Figure 18. Output spectrum of the 50-MHz punch-through varactor diode tripler.

5. CONCLUSIONS

Nonlinear reactive multipliers are the most efficient and stable multipliers over temperature. One type of nonlinear reactive multiplier is the punch-through varactor multiplier. A general theoretical description of the punch-through varactor multiplier was presented, as well as specific design information for a doubler and a tripler circuit. Higher order multipliers, as well as different circuit topologies for the doubler and tripler, can be built using the general theoretical description. To round off the discussion, examples of a doubler and tripler were shown with their results.

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APPENDIX A
DOUBLER EQUATIONS

A.1 GENERIC DOUBLER EQUATIONS

General Case		Lossless Case ($R_s = 0$)	
$D_2 = -4.713\frac{R_s\omega_o}{S_{max}} + \sqrt{\frac{22.21R_s^2\omega_o^2}{S_{max}^2} + 1}$	(57)	$D_2 = 1$	(58)
$R_{in} = R_s + 0.4244\frac{S_{max}D_2}{2\omega_o}$	(55)	$R_{in} = 0.2122\frac{S_{max}}{\omega_o}$	(60)
$R_{out} = -R_s + 0.8488\frac{S_{max}}{4\omega_o D_2}$	(54)	$R_{out} = 0.4244\frac{S_{max}}{2\omega_o}$	(59)
$\varepsilon(D_2) = \frac{0.8488S_{max}D_2 - 4R_sD_2^2\omega_o}{0.8488S_{max}D_2 + 4R_s\omega_o}$	(56)	$\varepsilon = 1$	

Implicit equation for t_{qmax}:

$\cos(\omega_o t_{q\max}) = -D_2\cos(2\omega_o t_{q\max})$	(62)	$t_{q\max} = \frac{\pi}{3\omega_o}$	(63)
$P_{in} = \frac{2V_{max}^2\omega_o^2\left[R_s + \frac{0.2122S_{max}D_2}{\omega_o}\right]}{S_{max}^2\left[2\sin(\omega_o t_{q\max}) + D_2\sin(2\omega_o t_{q\max})\right]^2}$	(64)	$P_{in} = 0.06287\frac{V_{max}^2\omega_o}{S_{max}}$	(65)

A.2 DOUBLER CIRCUIT DESIGN EQUATIONS

Figure A-1 illustrates the doubler circuit that relates to the equations in this section.

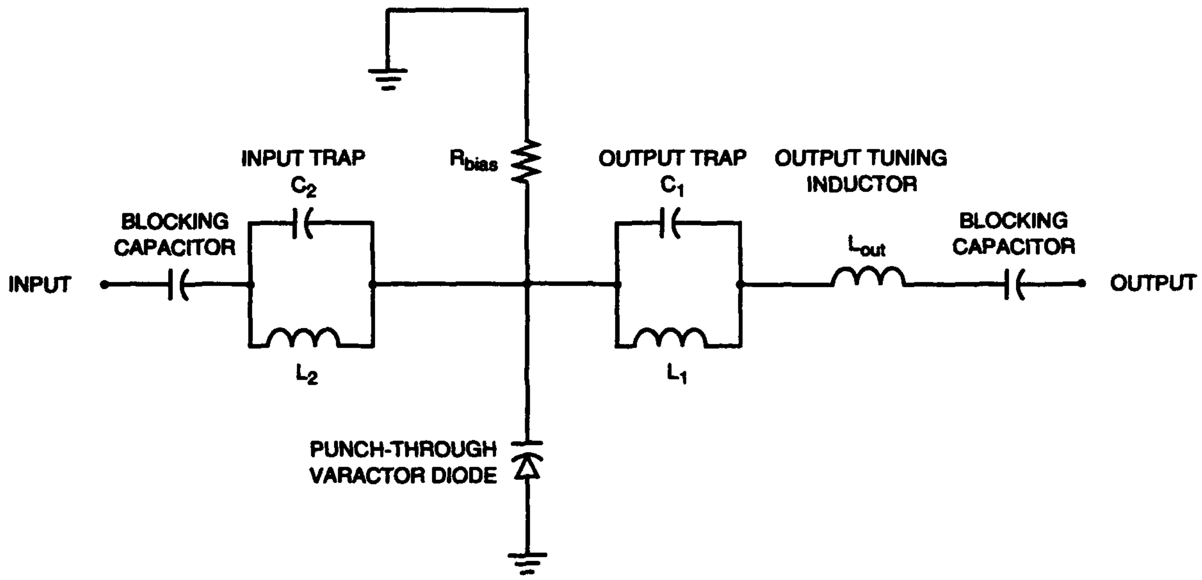

Figure A-1. Punch-through varactor diode doubler circuit.

$$C_{\min} = 0.03377 \frac{1}{Z_o f_o} \tag{89}$$

$$V_{\max} = 1.591 \sqrt{\frac{P_{\text{in}}}{f_o C_{\min}}} \tag{90}$$

$$R_{\text{bias}} = \frac{\tau}{C_{\min}} \tag{91}$$

$$C_2 = \frac{2}{3} C_{\min} \tag{92}$$

$$L_2 = \frac{1}{4\omega_o^2 C_2} \tag{93}$$

$$C_1 = \frac{8}{3} C_{\min} \tag{94}$$

$$L_1 = \frac{1}{\omega_o^2 C_1} \tag{95}$$

$$L_{\text{out}} = \frac{2}{3} L_1 \tag{96}$$

APPENDIX B
TRIPLER EQUATIONS

B.1 GENERIC TRIPLER EQUATIONS

General Case | **Lossless Case** ($R_s = 0$)

$$D_2 = -4.713\frac{R_s\omega_o}{S_{max}} \pm \sqrt{83.92\frac{R_s^2\omega_o^2}{S_{max}^2} - 26.19\frac{R_s\omega_o}{S_{max}} + 3.781} \quad (79)$$

$$D_2 = 1.944 \quad (80)$$

$$D_3 = 1.667 - \frac{7.854\omega_o D_2 R_s}{S_{max}} \quad (75)$$

$$D_3 = 1.667 \quad (76)$$

$$R_{in} = R_s + \frac{S_{max}}{2\omega_o}[0.4244 D_2] \quad (74)$$

$$R_{in} = 0.4125\frac{S_{max}}{\omega_o} \quad (82)$$

$$R_{out} = -R_s + \frac{S_{max}}{6\omega_o D_3}[0.7639 D_2] \quad (72)$$

$$R_{out} = 0.4454\frac{S_{max}}{3\omega_o} \quad (81)$$

$$\varepsilon(D_2, D_3) = \frac{0.1273 S_{max} D_2 D_3 - R_s D_3^2 \omega_o}{0.2122 S_{max} D_2 - R_s \omega_o} \quad (78)$$

$$\varepsilon = 1$$

Implicit equation for t_{qmax}:

$$0 = \cos(\omega_o t_{q\,max}) + D_2 \cos(2\omega_o t_{q\,max}) + D_3 \cos(3\omega_o t_{q\,max}) \quad (84)$$

$$t_{q\,max} = \frac{0.7295}{\omega_o} \quad (85)$$

$$P_{in} = \frac{2V_{max}^2\omega_o^2 R_s + 0.4244 V_{max}^2 \omega_o D_2 S_{max}}{S_{max}^2\left[\frac{2}{3}D_3\sin(3\omega_o t_{q\,max}) + D_2\sin(2\omega_o t_{q\,max}) + 2\sin(\omega_o t_{q\,max})\right]^2} \quad (86)$$

$$P_{in} = 0.04742\frac{V_{max}^2\omega_o}{S_{max}} \quad (87)$$

B.2 TRIPLER CIRCUIT DESIGN EQUATIONS

Figure B-1 illustrates the tripler circuit that relates to the equations in this section.

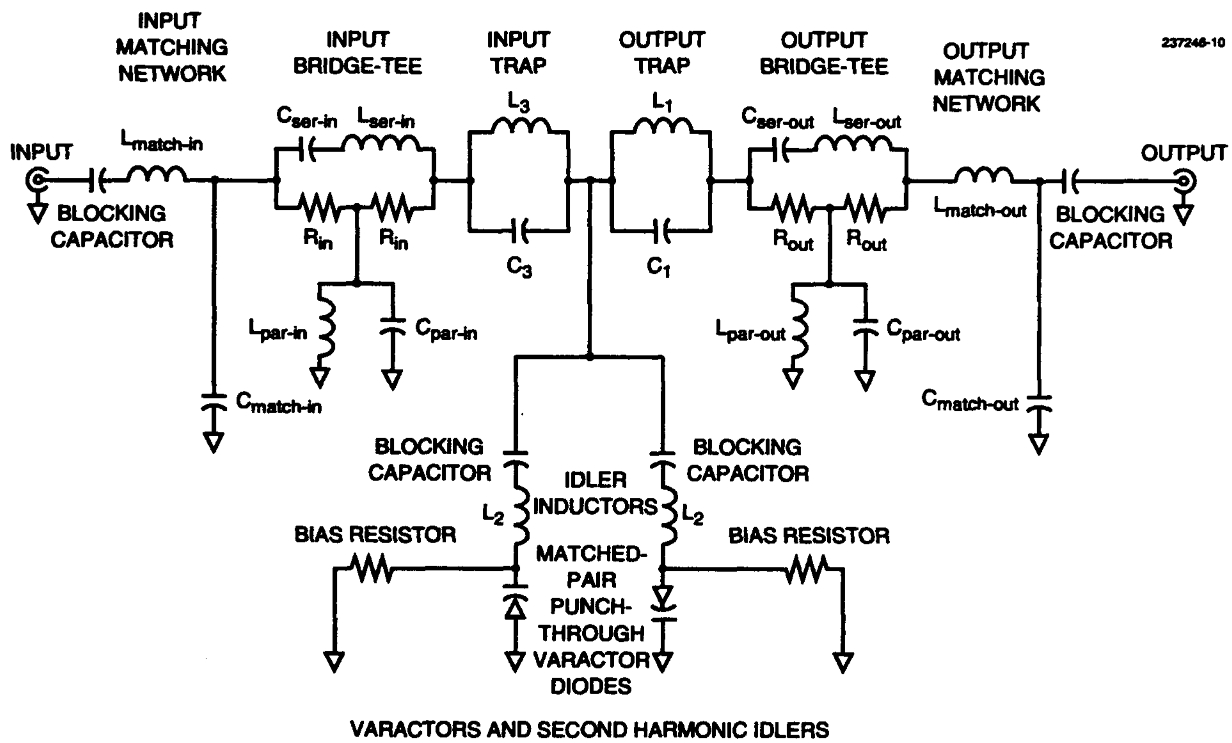

Figure B-1. Punch-through varactor diode tripler circuit.

$$R_{\text{in}} = \frac{5}{3} Z_o \quad \text{and} \quad R_{\text{out}} = \frac{3}{5} Z_o \tag{98}$$

$$C_{\min} = 0.03283 \frac{1}{f_o R_{\text{in}}} \tag{99}$$

$$L_2 = \frac{1}{8\omega_o^2 C_{\min}} \tag{100}$$

$$V_{\mathrm{max}} = 0.916\sqrt{\frac{P_{\mathrm{in}}}{f_{\mathrm{o}} C_{\mathrm{min}}}} \tag{101}$$

$$R_{\mathrm{bias}} = \frac{\tau}{C_{\mathrm{min}}} \tag{102}$$

$$L_{\mathrm{ser-in}} = \frac{R_{\mathrm{in}} Q_{\mathrm{in}}}{\omega_{\mathrm{o}}} \qquad C_{\mathrm{ser-in}} = \frac{1}{\omega_{\mathrm{o}} R_{\mathrm{in}} Q_{\mathrm{in}}} \tag{103}$$

$$L_{\mathrm{par-in}} = \frac{R_{\mathrm{in}}}{Q_{\mathrm{in}} \omega_{\mathrm{o}}} \qquad C_{\mathrm{par-in}} = \frac{Q_{\mathrm{in}}}{\omega_{\mathrm{o}} R_{\mathrm{in}}} \tag{104}$$

$$L_{\mathrm{ser-out}} = \frac{R_{\mathrm{out}} Q_{\mathrm{out}}}{3\omega_{\mathrm{o}}} \qquad C_{\mathrm{ser-out}} = \frac{1}{3\omega_{\mathrm{o}} R_{\mathrm{out}} Q_{\mathrm{out}}} \tag{105}$$

$$L_{\mathrm{par-out}} = \frac{R_{\mathrm{out}}}{Q_{\mathrm{out}} 3\omega_{\mathrm{o}}} \qquad C_{\mathrm{par-out}} = \frac{Q_{\mathrm{out}}}{3\omega_{\mathrm{o}} R_{\mathrm{out}}} \tag{106}$$

$$L_3 = \frac{4}{3} L_2 \qquad C_3 = \frac{2}{3} C_{\mathrm{min}} \tag{107}$$

$$L_1 = \frac{20}{9} L_2 \qquad C_1 = \frac{18}{5} C_{\mathrm{min}} \tag{108}$$

$$L_{\mathrm{match\text{-}in}} = \frac{Z_o}{\omega_o} \sqrt{\frac{R_{\mathrm{in}}}{Z_o} - 1} \qquad C_{\mathrm{match\text{-}in}} = \frac{\sqrt{\frac{R_{\mathrm{in}}}{Z_o} - 1}}{\omega_o R_{\mathrm{in}}} \tag{109}$$

$$L_{\mathrm{match\text{-}out}} = \frac{R_{\mathrm{out}}}{3\omega_o} \sqrt{\frac{Z_o}{R_{\mathrm{out}}} - 1} \qquad C_{\mathrm{match\text{-}out}} = \frac{\sqrt{\frac{Z_o}{R_{\mathrm{out}}} - 1}}{3\omega_o Z_o} \tag{110}$$

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13. ABSTRACT (*Maximum 200 words*)

Punch-through varactor diode frequency multipliers, a type of nonlinear reactive multiplier, can be 100% efficient, theoretically. This report presents a model of a punch-through diode and then analyzes it in the frequency domain. By restricting the currents that can flow, the analysis can be reduced to a finite set of equations for any order multiplier. Next, assuming that the diode loss is low enough, diode equations for the specific cases of a doubler and a tripler are developed. The report then adds the necessary circuit elements to give lumped-element circuit designs and design equations for both doublers and triplers. Finally, sample circuits are built using these designs, and design equations are shown along with their performance.

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